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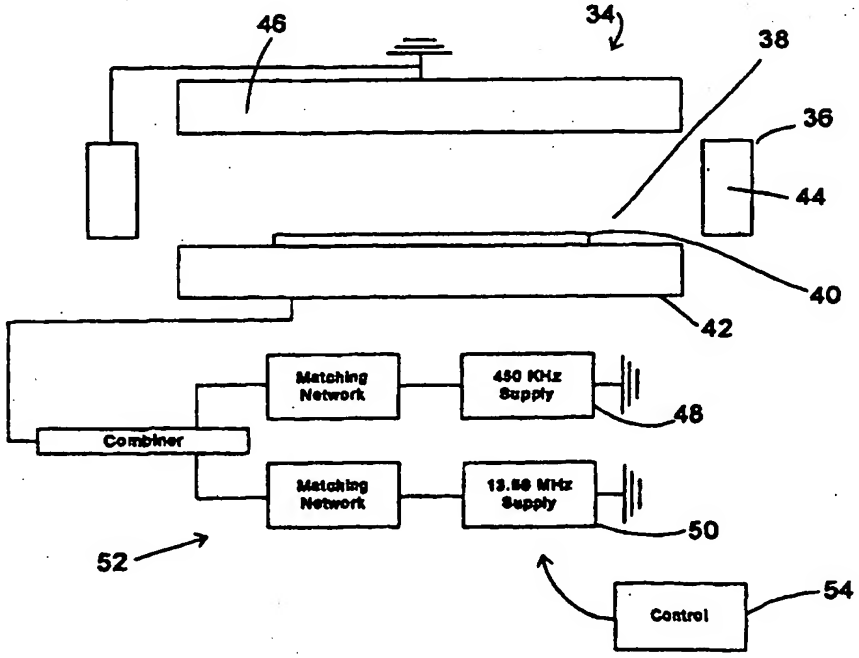
(54) Title: METHOD AND APPARATUS FOR ETCHING A SEMICONDUCTOR WAFER



(57) Abstract

A method and apparatus (6) provides for etching a semiconductor wafer (40) using a two step physical etching and chemical etching process in order to create vertical sidewalls (20) required for high density DRAMs and FRAMs.

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METHOD AND APPARATUS FOR ETCHING A SEMICONDUCTOR WAFER

This application is a continuation-in-part of Serial No. 08/675,559 filed July 3, 1996, and Serial No. 08/675,093, filed July 3, 1996.

Cross-Reference:

The following U.S. patent applications, all owned by Tegal Corporation, are cross-referenced and hereby incorporated by reference:

1. Title: INTEGRATED SEMICONDUCTOR WAFER PROCESSING SYSTEM
   Inventor: Stephen P. DeOrnellas
   Serial No.: 08/438,261
   Filed: May 10, 1995
   Docket No.: TEGL 1003 SRM

2. Title: PLASMA ETCH REACTOR AND METHOD
   Inventor: Stephen P. DeOrnellas
   Leslie G. Jerde
   Alferd Cofer
   Robert C. Vail
   Kurt A. Olson
   Serial No.: 08/675,559
   Filed: July 3, 1996
   Docket No.: TEGL 1008 SRM

3. Title: PLASMA ETCH REACTOR AND METHOD FOR EMERGING FILMS

Inventor: Stephen P. DeOrnellas
Alferd Cofer
Robert C. Vail

Serial No.: 08/675,093
Filed: July 3, 1996
Docket No.: TEGL 1009 SRM

Field of the Invention:

The present invention is directed to an improved plasma etch reactor apparatus and method.

Background of the Invention:

A new set of emerging films are being beneficially employed in the development of high density semiconductor chips such as for example high density dynamic random access memories ("DRAM") and ferroelectric random access memories ("FRAM"). These materials provide for higher capacity devices by allowing for a reduction in the size of the individual features on the memory substrate. Accordingly, enhanced profile control technologies are required.

In the past, a number of techniques have been used to obtain a desired semiconductor feature wall profile. One technique is ion milling which is classified as a physical etching method. With this technique, an ion mill beam is used to physically sputter away portions of a layer of a semiconductor device which are not desired, leaving the desired feature defining the various components and traces on the semiconductor device. While such techniques have produced desirable profiles, the disadvantage of using ion milling techniques is that the

processes are slower and such techniques tend to cause the formation of veils or fences upstanding from the desired feature.

Photoresist material is to protect and define the desired features produced by the ion milling technique. Once the photoresist material is stripped away, the veils or fences remain as undesirable and difficult to remove structures.

Chemical etching is another technique employed to remove portions of a layer of a semiconductor wafer which are unprotected by photoresist material. Such methods, while providing for faster etching than provided by, for example, ion milling, do not necessary have the same profile control afforded by ion milling.

Accordingly, there is a need to provide an etching process and apparatus which quickly and accurately processes emerging films which are used in the latest semiconductor products.

Summary of the Invention:

The present invention includes a method and apparatus designed to process emerging films which present unique etch problems. Such new films include for example, platinum and barium strontium titanate (BST), which are currently being used in the development of high density DRAM devices, and platinum and lead zirconium titanate (PZT) or bismuth strontium tantalate (Y-1), which are currently being used in development of non-volatile, FRAM devices. Of these new films, BST, PZT, and Y-1 have for example a high dielectric constant which allows for the development of greater circuit density, fine line geometry devices. With enhanced feature densities, more exacting vertical profile are required.

The present invention is directed to performing critical etching which results in anisotropic profiles (i.e., straight, vertical sidewalls) which is highly selective and causes minimal damage to the underlayer

or other wafer materials, and which is performed uniformly over a non-uniform area.

Accordingly, the present invention provides for an apparatus and method which allows for a physical etching and then a chemical etching of a wafer in order to obtain wafer features with highly advantageous vertical sidewall profiles. The present invention provides for a method and apparatus which operates on a continuum, first emphasizing physical etching such as for example, by way of ion milling, and then emphasizing chemical etching.

Such a technique is uniquely counter-intuitive in that the ion milling portion of the process creates the desired vertical profiles, but in addition creates undesirable veils. However, advantageously, the present invention provides for a chemical etching in a continuum with the operation, which chemical etching satisfactory removes the veils. Accordingly thereafter, such that the semiconductor wafer can be operated on with other methods such as the unique rinse-strip-rinse method presented in the above U.S. Patent Application No. 08/438,261, to obtain the desired feature, configuration, densities and profiles. Thus, after the chemical etching process has occurred, the wafer is rinsed in order to remove any soluble residue prior to the stripping away of the photoresist material in a stripping or ashing step and with a subsequent post-strip rinsing of the semiconductor wafer to remove residue.

The method is performed in a chamber which has an electrode adjacent to where the semiconductor wafer is placed. The electrode is provided with a first power supply operated in the megahertz range and with a second power supply operated in the kilohertz range. During the first portion of the method, both power supplies are operable in order to enhance the ion milling technique. During the second portion of the method where the chemical etching is

predominant, the second power supply operating in the kilohertz range is turned off, greatly reducing the influence of ion milling.

In another feature of the invention, a tri-electrode chamber is used wherein the bottom electrode is located adjacent the wafer and is powered as indicated above with two power supplies. A side peripheral electrode is either grounded or free-floating, and a top electrode spaced from and locked above the wafer is either grounded or allowed to be free-floating.

Other features, objects and advantageous of the invention can be obtained from a review of the specification, the claims, and the figures.

Brief Description of the Figures:

Fig. 1 is a micrograph of a semiconductor wafer feature using an ion milling technique showing the veils or fences and with the photoresist in place.

Fig. 2 is a micrograph of another semiconductor feature showing in greater detail the veils or fences remaining after an ion milling process and with the photoresist material removed.

Fig. 3 is a schematical representation of a feature such as found in Fig. 2 with the photoresist still in place.

Fig. 4 is a micrograph of a semiconductor feature including the photoresist after a typical chemical etching operation.

Fig. 5 is a schematical representation of a feature such as found in Fig. 4 with the photoresist still in place.

Fig. 6 is a schematical representation of an embodiment of the etching apparatus of the invention.

Fig. 7 is a micrograph of a feature of a semiconductor chip after the inventive physical and chemical etching steps of the invention have been performed.

Fig. 8 is a micrograph of the feature of Fig. 7 after an ashing or stripping step has been performed in order to remove photoresist material and residues.

Fig. 9 is a micrograph of the semiconductor feature of Fig. 8 after a rinse step has been performed in order to define the final desired feature with appropriate vertical profiles.

Fig. 10 is a schematical representation of the semiconductor feature shown in Fig. 7 with the photoresist material still in place.

Fig. 11 is a representative graph depicting the veil height remaining in comparison to a chlorine flow rate for the chemical etching process.

Fig. 12 is a graph showing ion energy and ion density compared to RF frequency at which the power supply is provided.

Fig. 13 is a top plan view of a wafer processing apparatus.

Detailed Description of the Preferred Embodiment:

As indicated above, improved profiles are important with the new emerging high density DRAMs and FRAMs which have fine line geometry with dense feature topography. The density of the features can be measured by the pitch, where the pitch is defined as sum of the width of the feature and the width of the space between features. Typically, high density features have a pitch which is about and less than 2.0 microns and preferably about and less than 0.5 microns. Features with such pitch are made possible using the present invention and also using high dielectric emerging films, such as lead zirconium titanate (PZT), barium strontium titanate (BST), and bismuth strontium tantalate (Y-1), which dielectric films have dielectric constants in the above 200 range, and typically between 200 and 1,400.

Such high density, emerging semiconductor structures employ material such as platinum (Pt), iridium (Ir), iridium dioxide (IrO_2), lead

zirconium titanate (PZT), ruthenium (Ru), ruthenium dioxide (RuO_2), barium strontium titanate (BST), bismuth strontium tantalate (Y-1), and other emerging films. For a high density feature the electrodes can be comprised of, for example, platinum with PZT (having a dielectric constant of about 1,400) or BST or Y-1 deposited therebetween in order to establish the high capacitive value required. To take maximum advantage of the ability to create such high capacitive features in a smaller space, it is important that the features have a profile in the range of 70° to 85° and preferably as close to normal as possible, and that there be no residues on the sidewalls.

With respect to Figs. 1, 2 and 3, micrographs and a schematic of a feature of a semiconductor wafer demonstrating vertical sidewalls with sidewall veils or fences extending upwardly therefrom are depicted. These veils 20 (Fig. 3) are caused by an ion milling process where sputtering dominates the etching process. Materials sputter from the areas unprotected by the photoresist 22 deposit as said veils 20. As can be seen in Fig. 3, these veils 20 tend to coat the photoresist material 22. When the photoresist material is stripped away, the veils remain as shown in Fig. 2. These veils are comprised of platinum from the platinum layer 24 which as shown in Fig. 3 has been deposited on the layer of titanium 26. These veils are redeposits of sputtered platinum and can include other materials such as silicon dioxide, carbon, halogens, and other materials involved in the etching process. These veils can also include materials from other films and layers which are contained in the semiconductor wafer, such as by way of example only, Ir, IrO_2, PZT, Ru, RuO_2, BST, and Y-1. It is to be understood that veils caused by ion milling are more prevalent for small pitch patterns, where the pitch is less than 0.5 microns, and thus the above process is most beneficial for the emerging high density DRAM

and FRAM devices. The advantage of this operation is the fact that the sidewalls produced are vertical in the 70° to 85° range and higher.

Figs. 4 and 5 depict the profile of a semiconductor feature produced through a chemical etch process. As can be seen in Fig. 5 the sidewall 28 of the platinum feature 30 has a poor profile, not suitable for dense patterns required for the above referenced advanced semiconductor devices. Chemical etching giving a sidewall profile of 40° to 50°. In both Figs. 4 and 5, the photoresist material 32 is positioned atop the platinum layer 30, which layer has not been stripped away.

The present invention provides for a continuous etching operation using the benefits of both physical etching (ion milling) and chemical etching in order to produce a semiconductor feature having a profile such as shown in Fig. 10. The present invention includes an etching apparatus (tri-electrode reactor) 34 as seen in Fig. 6. The etching apparatus 34 includes a housing 36 and an etching chamber 38. A wafer 40 is positioned on a bottom electrode 42. The chamber 38 further includes side peripheral electrode 44 and an upper electrode 46. In a preferred embodiment, the side peripheral electrode 44 can be grounded or allowed to establish a floating potential as a result of the plasma developed in the chamber 38. The upper electrode 46 is generally grounded. In typical operation, both the side peripheral electrode 44 and the upper electrode 46 are grounded as shown in Fig. 6.

Preferably two power supplies, first power supply 48 and second power supply 50, are connected to the bottom electrode 42 through a appropriate circuitry 52 which includes matching networks and a combiner. Further a controller 54 controls the sequencing of the first and second AC power supplies 48, 50. Typically, the first power supply operated in the kilohertz range and is optimally provided at

about 450 KHz, and typically in the range of less than 500 KHz. The second power supply operates in the megahertz range, and typically operates at about 13.56 MHZ, although other frequencies above about 1 MHZ and also multiples of 13.56 MHZ can be used with the present invention. As can be seen in Fig. 12, ion energy increases towards the kilohertz range while ion density increases towards the megahertz range. This characteristic is important in the operation of the present invention as described below.

As indicated above, the present invention provides for a continuum of etching starting from predominantly physical etching (ion milling) and continuing to predominantly chemical etching. Such a procedure is quite naturally counter-intuitive as the first portion of the process requires physical etching, which physical etching has historically resulted in sidewall veils as shown in Fig. 3. Once the first step of physical etching is complete as measured by the process being within a certain range of or at end point, the process is converted to the second step of chemical etch through the introduction of a different gas regime with a different power input. The second step is effective in etching away the veils while maintaining the sidewall profile so that a semiconductor feature such as shown in Figs. 7 and 10 is established. In Fig. 10, the platinum layer 70 has substantially vertical sidewalls, and the platinum layer 70 and the photoresist layer 72 has substantially no veils associated therewith. Preferably, subsequent to the chemical etch operation, the semiconductor wafer is rinsed prior to a photoresist stripping operation so that water soluble compounds such as water soluble chlorides can be washed away prior to the photoresist stripping or ash operation. After the photoresist stripping operation, a post strip solvent rinse operation is performed. These steps are depicted in Figs. 7, 8 and 9 and will be discussed hereinbelow. These steps are also discussed in the above-referenced

patent application entitled INTEGRATED SEMICONDUCTOR WAFER PROCESSING SYSTEM which is directed to a proprietary rinse-strip-rinse operation and which is incorporated herein by reference.

It must be understood that in the preferred operation, during the first of physical etching, that chemical etching does occur, and also during the second step which is predominantly chemical etching that physical etching or ion milling also occurs.

By way of example, in a procedure for the inventive method, ion milling would be accomplished using argon and chemical etching would be accomplished using chlorine. In the first preferred method during the physical etching (ion milling) stage, argon would be supplied to the chamber 38 (Fig. 6) at about approximately 10 SCCM (standard cubic centimeter per minute) to about 50 SCCM and preferably at about 20 SCCM, and the chlorine would be supplied to the chamber at from about 2 SCCM to about 50 SCCM and preferably in the range of about 5 SCCM to about 10 SCCM. The pressure in the chamber during physical etch would be maintained at approximately 2 to 10 millitorr and preferably at about 5 millitorr with the temperature at approximately 80° C. Preferably the first power supply 48 would be operated at about 450 KHz in the power range of about 50 watts to about 200 watts. The second power supply 50 would be operated at about 13.56 MHZ in the power range of about 500 watts to about 1100 watts. Typically, the physical etching operation would run with a time period of about two-thirds to 100% of end point. The optical end point for a platinum structure where the platinum is 1000 angstroms thick would be approximately 70 seconds for a wafer in the 6" to 8" range. Optical end point for such a structure where the platinum is 2000 angstroms thick would be approximately 150 seconds for a wafer in the 6" to 8" range. When end point is used as a time measure, a trial physical etch process is run until end point is

reached. Thereafter, production runs are made based on a fraction of the end point time determined in the trial run. Alternatively, the timing for the physical etch operation can be obtained without determining end point. For example, the time period required to etch through a film can be determined and then a fraction of that time period, from by way of example only, about two-third to about one hundred percent of that time period, can be used for the physical etch step.

Once end point or a percentage of end point has been reached, the process shifts to predominantly chemical etching. In this situation, the argon is preferably maintained at about 20 SCCM and the chlorine flow rates increased preferably to about 15 SCCM. For chemical etch, however, the argon gas can have a flow rate of about zero SCCM to about 50 SCCM and the chlorine gas can have a flow rate of about 5 SCCM to about 100 SCCM.

Fig. 11 shows a graph comparing final veil height in angstroms to chlorine flow rates in SCCMs. As the flow rate for the chlorine increases, the veil height decreases and as can be seen with the flow rate at or above about 10 SCCM, the veil is substantially attacked and reduced in size. In the graph of Fig. 11 the line identified by 60 is for veils which are facing an open area. The line 62 is for veils with the features spaced at approximately 0.8 microns. Line 64 represents veils with features spaced at approximately 0.3 microns.

During the chemical etching operation, the pressure is reduced to approximately 2 millitorr to about 10 millitorr and preferably about 2 millitorr. The first power supply 48 in the kilohertz range is preferably turned off in order to significantly reduce the ion milling effect. In practice during chemical etch, the first power supply can operate in the range of about 0 watts to about 50 watts. As seen in Fig. 12, it is the kilohertz range power supply which drives ion milling operation by increasing the ion energy. The second power supply 30

is maintained at about 13.56 MHZ, with a power of about 500 watts to about 1100 watts.

In a preferred embodiment, for the second chemical etching phase of this two step operation, the chemical etch process is operated for a platinum thickness of both 1000 angstroms and 2000 angstroms for about 45 seconds to about 120 seconds in order to substantially remove the veils created through the ion milling process.

For etching of metals or conductors, chemistries including (1) argon and chlorine, (2) argon, chlorine and hydrogen bromide (HBr), or (3) argon, chlorine and carbonyl gases, (4) any of the above chemistries with oxygen (O_2), (5) SF_6 by itself or with any of the above chemistries, (6) NF_3 by itself or with any of the above chemistries, and (7) a fluorocarbon (CxFy) by itself or with other chemistries, are preferred. For etching oxides or dielectrics, chemistries can include combinations such as (1) argon and CF_4, (2) argon, CF_4, and chlorine, (3) argon, CHF_3, and chlorine, (4) any of the above combined with hydrogen bromide (HBr), (5) SF_6 by itself or with any of the above chemistries, (6) NF_3 by itself or with any of the above chemistries, (7) a fluorocarbon (CxFy) by itself or with other chemistries, and (8) argon and chlorine gases.

The results of the above two step process, both the physical etching and the chemical etching, are seen in micrograph of Fig. 7 where the photoresist is identified by the central peak of each feature and some remnants of the veils are shown on each side thereof. At this stage, the semiconductor feature is rinsed in order to remove any soluble compounds. After rinsing, the semiconductor wafer is exposed to a stripping or ashing process in order to remove the photoresist and residue associated with the veils (Fig. 8). The stripping operation is performed preferably with a wet solvent. The solvent attacks both the remaining veils and the photoresist. After the stripping operation, the

semiconductor wafer is exposed to a subsequent rinsing operation resulting in the feature as indicated in Fig. 9.

The rinse-strip-rinse operation, as indicated above, can be carried out by way of example by the apparatus as shown in Fig. 13. The system of Fig. 13 includes a vacuum load lock chamber 116, an alignment module 118, two etch modules 120 and 122, and a strip module 124, all of which are connected to a central vacuum chamber 126 through a closable opening and are operated by a computer process control system (not shown). Load lock chamber 116 houses an internal cassette elevator for holding a wafer cassette (entry cassette). Vacuum chamber 126 has a robotic wafer handling system 138 for transferring wafers from one chamber or module to another. Strip module 124 is connected to an atmospheric robotic wafer handling system 132 through a closable opening 127, which in turn is connected to rinse module 125 and atmospheric cassette module 134 (exit cassette). An example of a typical rinse module used is the Semitool Equinox rinse system. Atmospheric robotic wafer handling system 132 services the atmospheric cassette module 134 which holds wafers after the completion of processing. In addition, the second robotic wafer handling system 132 transfers wafers between strip module 124 and rinse module 125. During the rinsing process, rinse module 125 and robotic handling system 132 are designed to maintain the degree of wafer alignment required by strip module 124 for stripping. The operation of the present invention is automated and programmable through a computing system.

In operation, after being etched in one of the etching modules 120, 122, the wafer is transported through the strip module 124 to the rinse module 125 by the robotic arm 132 where the first rinse occurs. After this rinse, the robotic arm 132 transfers the wafer back to the strip module 124 where photoresist stripping occurs. After

stripping, the wafer is then transported by the robotic arm 32 back to the rinse module 25 for final rinsing.

It is to be understood that the present invention can also be used with hard masks (oxides and the like) as well as with composite structures with photoresist. The invention additionally can be used with a wide range of films in addition to the emerging films specified herein.

It is also to be appreciated that reactors other than that specified above can be used with the method. By way of example only, the present invention can be used with inductively coupled plasma source reactors (ICP). Inductively coupled plasma sources can include by way of example only helicon reactors and helical reactors. The above tri-electrode reactor is a capacitively coupled reactor. Further, the present method can be used in a reactor that is both inductively coupled and capacitively coupled. Other reactors such as ECRs, electron cyclotron resonance reactors can be used with the present invention.

Industrial Applicability:

From the above, it can be seen that the present inventive apparatus and method provides an etching operation including first a physical etching step and then a second chemical etching step in order to accomplish the desired vertical profiles for density patterns on semiconductor wafers required by the emerging DRAMs and FRAMs. This inventive apparatus and method allows the vertical walls to be established and then the veils to be removed. The apparatus and method are capable of handling the new emerging films required for the newest high density semiconductor products.

Other features, aspects and objects of the invention can be obtained from a review of the figures and the claims.

It is to be understood that other embodiments of the invention can be developed and fall within the spirit and scope of the invention and claims.

We claim:

1. A method of etching a wafer comprising the steps of:

physically etching and then chemically etching a wafer in order to obtain wafer features with at least substantially vertical side wall profiles.

2. The method of claim 1 including the step of:

wherein said steps of physically etching and then chemically etching provide for substantially vertical side wall profiles with less residue.

3. The method of claim 1 wherein the step of physically etching the wafer uses argon gas at about 10 SCCM to about 50 SCCM and chlorine gas at about 2 SCCM to about 50 SCCM.

4. The method of claim 1 wherein the step of physically etching the wafer occurs at about 2 millitorr to about 10 millitorr.

5. The method of claim 1 wherein said step of physical etching occurs in a chamber with the wafer positioned adjacent to an electrode which is provided with power at about 450 KHz and with power at about 13.56 MHZ.

6. The method of claim 1 wherein said step of physical etching occurs in a chamber with the wafer positioned adjacent to an electrode, which electrode is provided with a first power source at about or less than 500 KHz and with a second power source at about one MHZ or greater.

7. The method of claim 1 wherein said step of physical etching occurs in a chamber with the wafer positioned on the electrode, which electrode is provided with a first power supply operated in a kilohertz range and a second power supply operated in a megahertz range.

8. The method of claim 7 wherein said first power source provides power in the range of about 50 watts to about 200 watts and said second power source provides power in the range of about 500 watts to about 1100 watts.

9. The method of claim 7 wherein said electrode is a bottom electrode and said method is performed in a chamber which also has a side peripheral electrode located adjacent to an edge of the bottom electrode and an upper electrode that is above and spaced from the bottom electrode and wherein said side peripheral electrode is one of electrically grounded or electrically floating, and said upper electrode is one of electrically grounded or electrically floating.

10. The method of claim 1 wherein said physical etching step is performed at about 80° C.

11. The method of claim 1 wherein said physical etching step is performed from between about two-thirds of the endpoint detection time and about endpoint detection time.

12. The method of claim 3 wherein the step of etching the wafer uses argon gas at about zero SCCM to about 50 SCCM and chlorine gas in the range of about 5 SCCM to about 100 SCCM.

13. The method of claim 4 wherein the step of chemically etching the wafer occurs at about 2 millitorr to about 10 millitorr.

14. The method of claim 7 wherein the step of chemical etching occurs with the electrode provided with from about no power to about 50 watts from the first power source operated in the kilohertz range and with power from the second power source operated in the megahertz range.

15. The method of claim 14 wherein during the step of chemical etching the second power source provides power in the range of about 500 watts to about 1100 watts.

16. The method of claim 7 wherein during the step of chemical etching the first power supply operated in the kilohertz range is turned off in order to reduce the effects from physical etching.

17. The method of claim 1 wherein for a layer of platinum at about 1000 angstroms thick the physical etching step takes about 70 seconds and the chemical etching step takes about 60 seconds to about 120 seconds, and for a layer of platinum at about 2000 angstroms thick the physical etching step takes about 150 seconds and the chemical etching step takes about 60 seconds to about 120 seconds.

18. The method of claim 1 wherein for metal layers the physical etching and the chemical etching use one of (1) argon and chlorine gases, (2) argon, chlorine, and hydrogen bromide gases, (3) argon, chlorine, and carbonyl gases, (4) any of the above with oxygen (O_2), (5) SF_6 by itself or with any of the above, (6) NF_3 by itself or with

any of the above chemistries, and (7) a fluorocarbon (CxFy) by itself or with other chemistries.

19. The method of claim 1 wherein for dielectric layers the physical etching and the chemical etching use one (1) argon and CF_4 gases, (2) argon, CF_4 and chlorine gases (3) argon, CHF_3 and chlorine gases, (4) any of the above combination with hydrogen bromide gases, (5) SF_6 by itself or with any of the above, (6) NF_3 by itself or with any of the above, (7) a fluorocarbon (CxFy) by itself or with other chemistries, and (8) argon and chlorine gases.

20. The method of claim 1 wherein there is an electrode which is provided with first power supply in the kilohertz range and with a second power supply in the megahertz range during physical etching and is provided with a power supply in the megahertz range during chemical etching.

21. A method of etching a wafer comprising the steps of:
creating veils on features of the wafer using ion milling; and
removing the veils with chemical etching.

22. The method of claim 23 including the step of performing the creating and the removing steps on materials including at least one of platinum, iridium, iridium oxide, ruthenium, ruthenium oxide, bismuth strontium tantalate, barium strontium titanate, and lead zirconium titanate.

23. The method of claim 23 including the step of performing the creating and removing steps on a high dielectric material.

24. The method of claim 23 including the step of performing the creating and the removing steps on a material that has a dielectric constant over 200.

25. A method of etching a wafer comprising the steps of:

creating a substantially vertical side wall profile on a feature of the wafer and side wall veils; and

removing the veils while leaving the substantially vertical side wall profile.

26. The method of claim 27 wherein said steps are for creating substantially vertical side wall profiles which are about equal to and greater than 70°.

27. The method of claim 27 wherein:

said creating step is accomplished using predominately physical etching; and

said removing step is accomplished using predominately chemical etching.

28. A method of etching a wafer comprising the steps of:

performing a combined physical etch and chemical etch of a wafer with the step being principally a physical etch step; and

subsequently performing a combined physical etch and chemical etch of the wafer with the subsequent step being principally a chemical etch step.

29. The method of claim 1 performed on a semiconductor wafer with a pitch of about or less than 2.0 microns and preferably less than 0.5 microns.

30. The method of claim 1 performed on fine line geometry semiconductor devices having a pitch of about or less than 2.0 microns and preferably less than 0.5 microns.

31. An apparatus for etching a semiconductor wafer including:

an etching chamber;

a first electrode;

a first power supply operating in the kilohertz range which is selectably connectable to the first electrode;

a second power supply operating in the megahertz range which is selectably connectable to the first electrode;

a second electrode spaced from the first electrode;

said wafer positionable adjacent to the first electrode; and

a controller that can selectively cause the first and the second power supplies to supply power to the first electrode during a physical etch operation and can selectively cause the second power supply operating in the megahertz range to supply power to the first electrode during a subsequent chemical etching operation while reducing the power output from the first power supply operating in the kilohertz range.

32. The apparatus of claim 33 wherein said second electrode is one of grounded or allowed to electrically float.

33. The apparatus of claim 32 including:

a side peripheral electrode which is located about a periphery of the first electrode between the first and the second electrode; and

wherein said side peripheral electrode is one of grounded or electrically floating.

34. The method of claim 3 wherein the step of physically etching the wafer uses argon gas at preferably about 20 SCCM and chlorine gas at about 5 SCCM to about 10 SCCM.

35. The method of claim 4 wherein the step of physically etching the wafer occurs preferably at about 5 millitorr.

36. The method of claim 8 wherein the first power source preferably provides power in the range of about 100 watts to about 200 watts and the second power source provides power in the range of about 500 watts to about 700 watts.

37. The method of claim 1 wherein the step of chemically etching the wafer uses argon gas at about zero SCCM to about 50 SCCM and chlorine gas in the range of about 5 SCCM to about 100 SCCM.

38. The method of claim 3 wherein the step of chemically etching the wafer preferably uses argon gas at about 20 SCCM and chlorine gas in the range of about 10 SCCM to about 15 SCCM.

39. The method of claim 37 wherein the step of chemically etching the wafer preferably uses argon gas at about 20 SCCM and chlorine gas in the range of about 10 SCCM to about 15 SCCM.

40. The method of claim 13 wherein the step of chemically etching the wafer occurs preferably at about 2 millitorr.

41. The method of claim 14 wherein the step of chemically etching occurs with the electrode provided with about no power from the first power source operated in the kilohertz range.

42. The method of claim 1 wherein the physical etching step is performed for a percentage of end point deflection time.

43. The method of claim 1 wherein the physical etching step is performed for a percentage of the time period required to etch through a film.

44. The method of claim 1 used in one of (1) an inductively coupled plasma source reactor, (2) an electron cyclotron resonance reactor, and (3) a tri-electrode reactor with high and low frequency power supplies coupled to one electrode.

45. The method of claim 1 used in a reactor that is both inductively coupled and capacitively coupled.

46. The method of claim 1 used in one of (1) an inductively coupled reactor and (2) a capacitively coupled reactor.

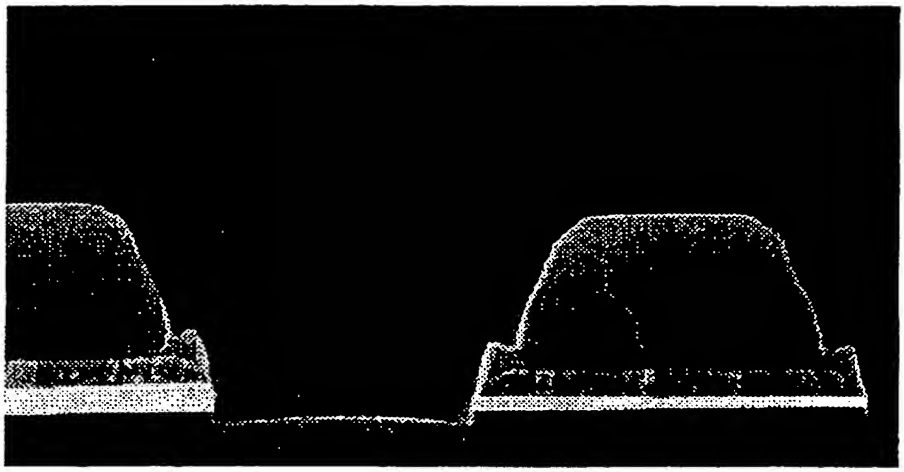

Fig. 1

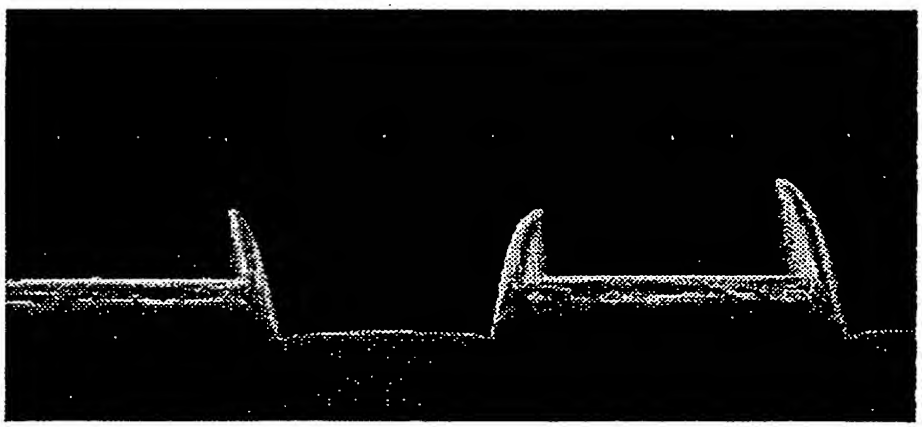

Fig. 2

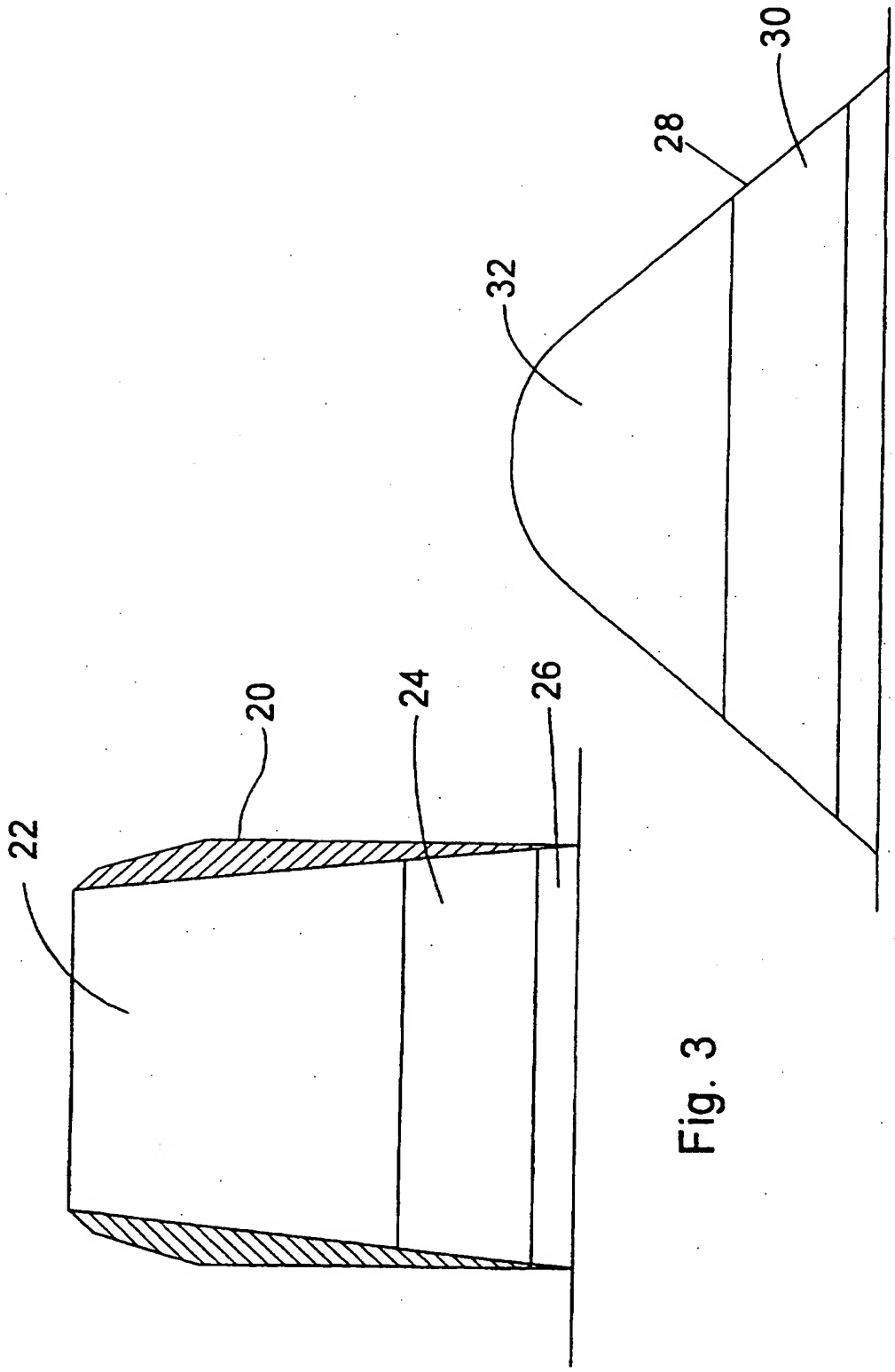

Fig. 3

Fig. 5

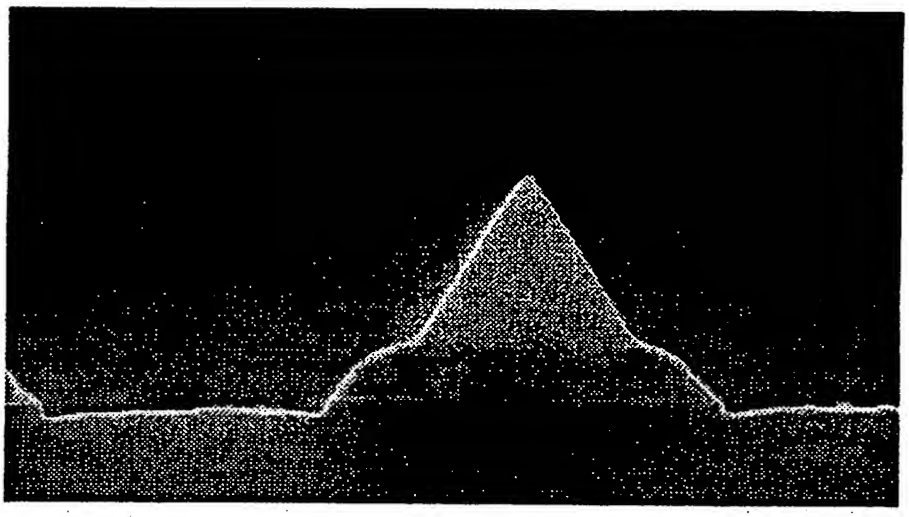

Fig. 4

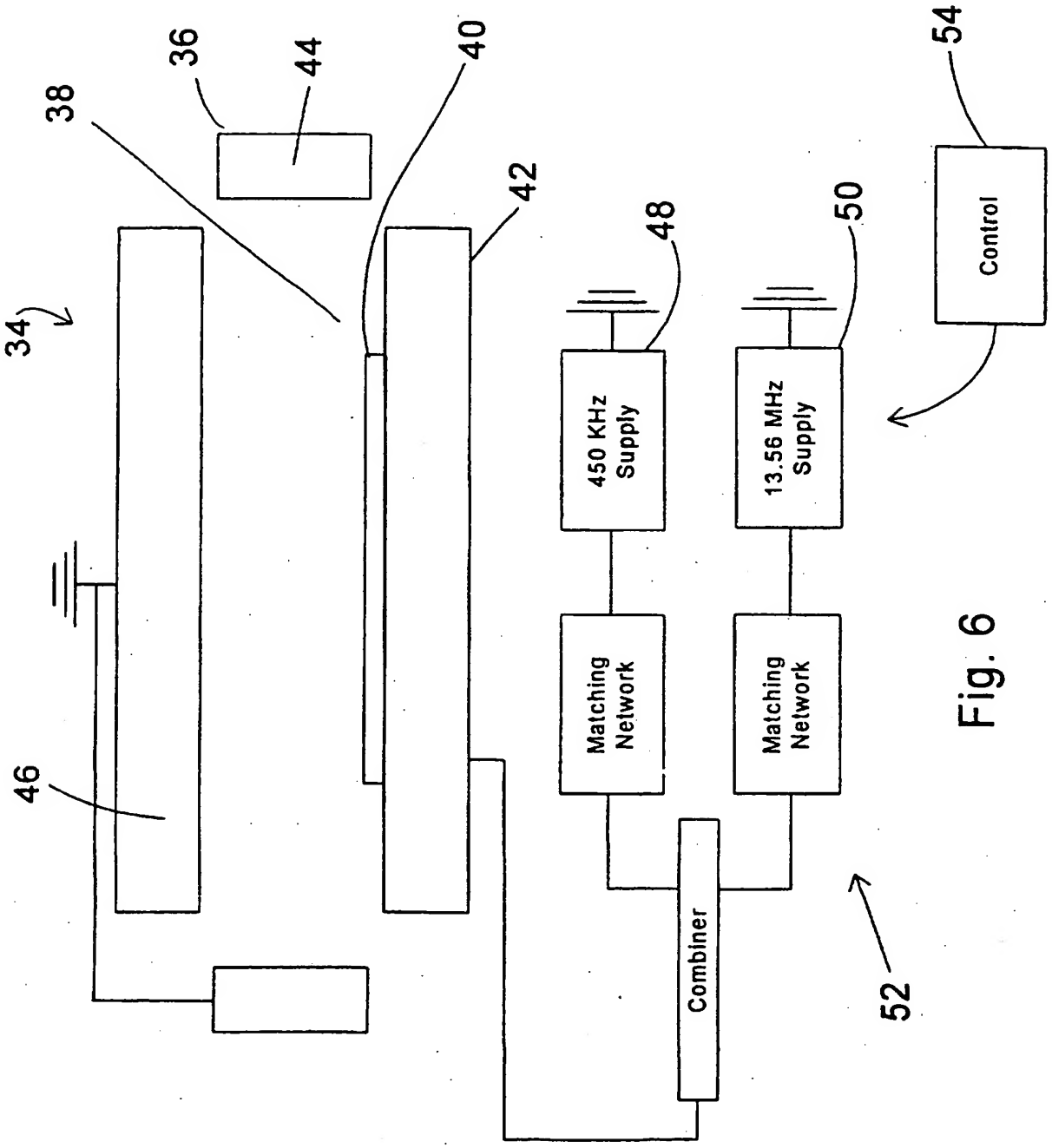
36
44
40
38
42
54
34
48
50
Control
450 KHz Supply
13.56 MHz Supply
Matching Network
Matching Network
46
Combiner
52

Fig. 6

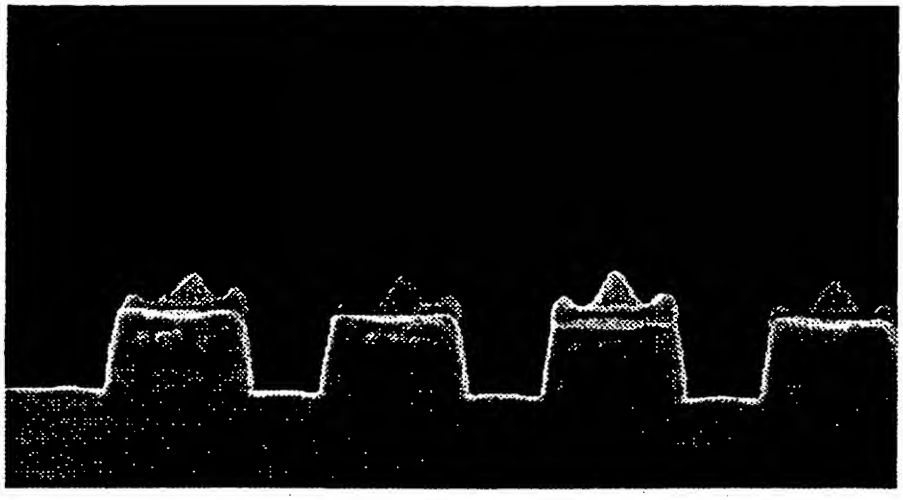

Fig. 7

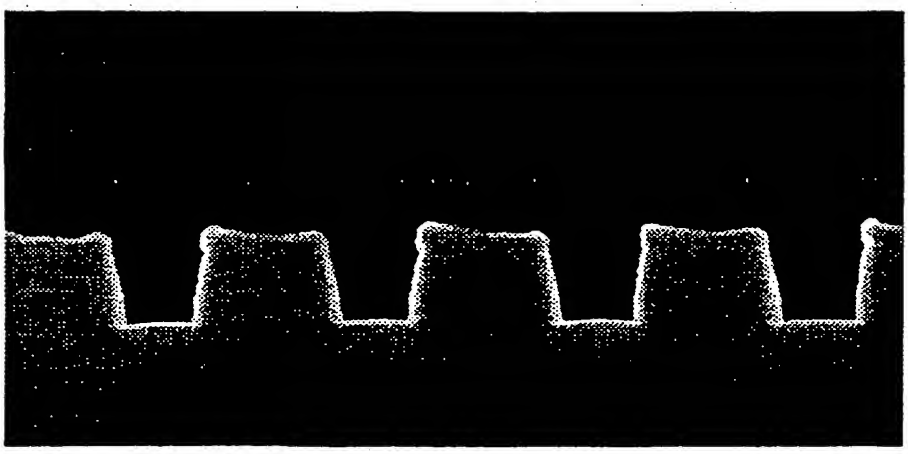

Fig. 8

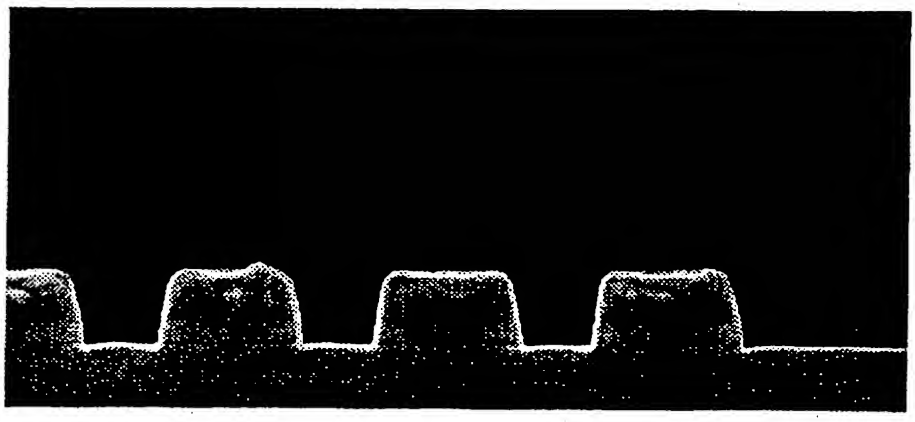

Fig. 9

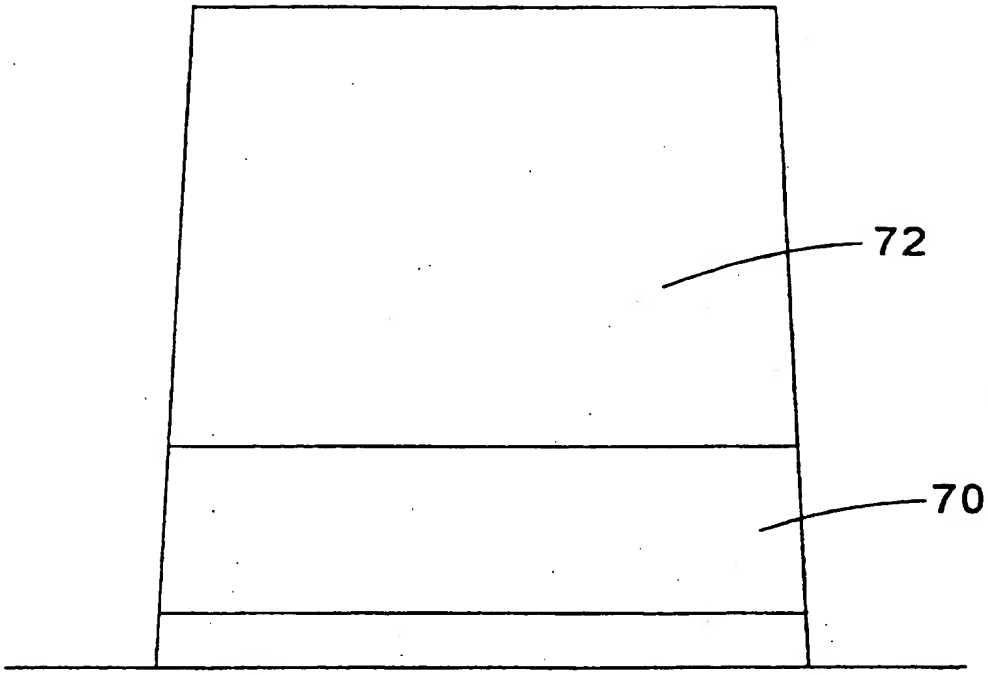

Fig. 10

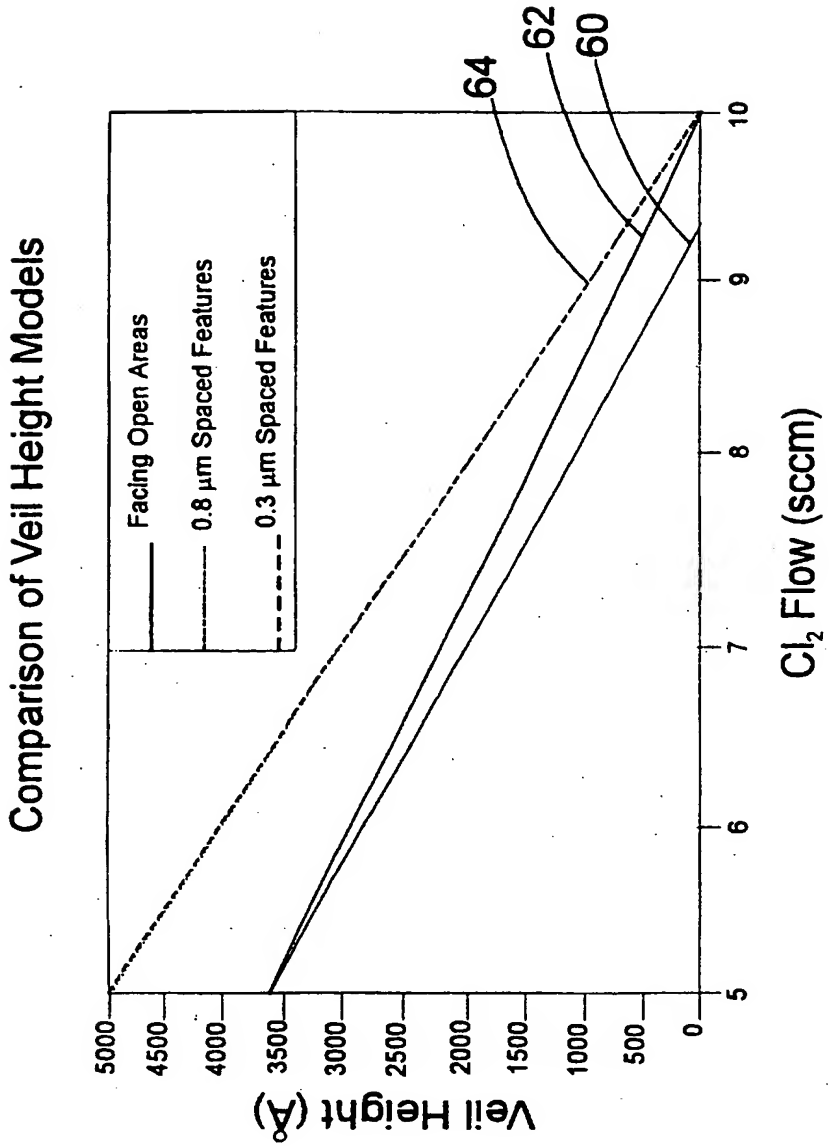
Comparison of Veil Height Models
Facing Open Areas
0.8 µm Spaced Features
0.3 µm Spaced Features
64
62
60
Veil Height (Å)
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
5
6
7
8
9
10
Cl2 Flow (sccm)

Fig. 11

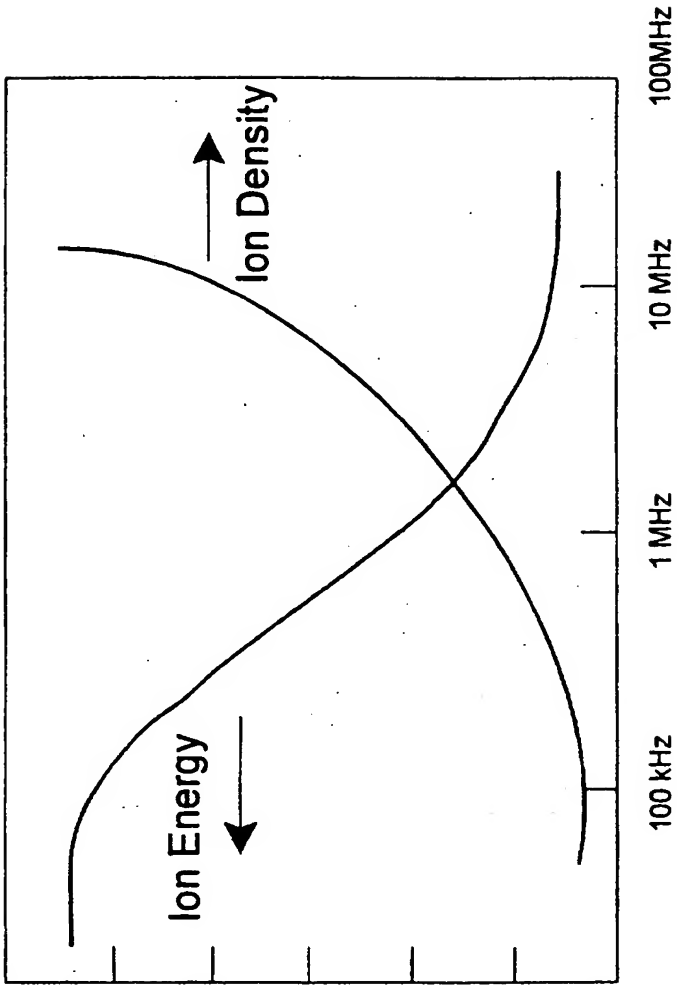

Fig. 12

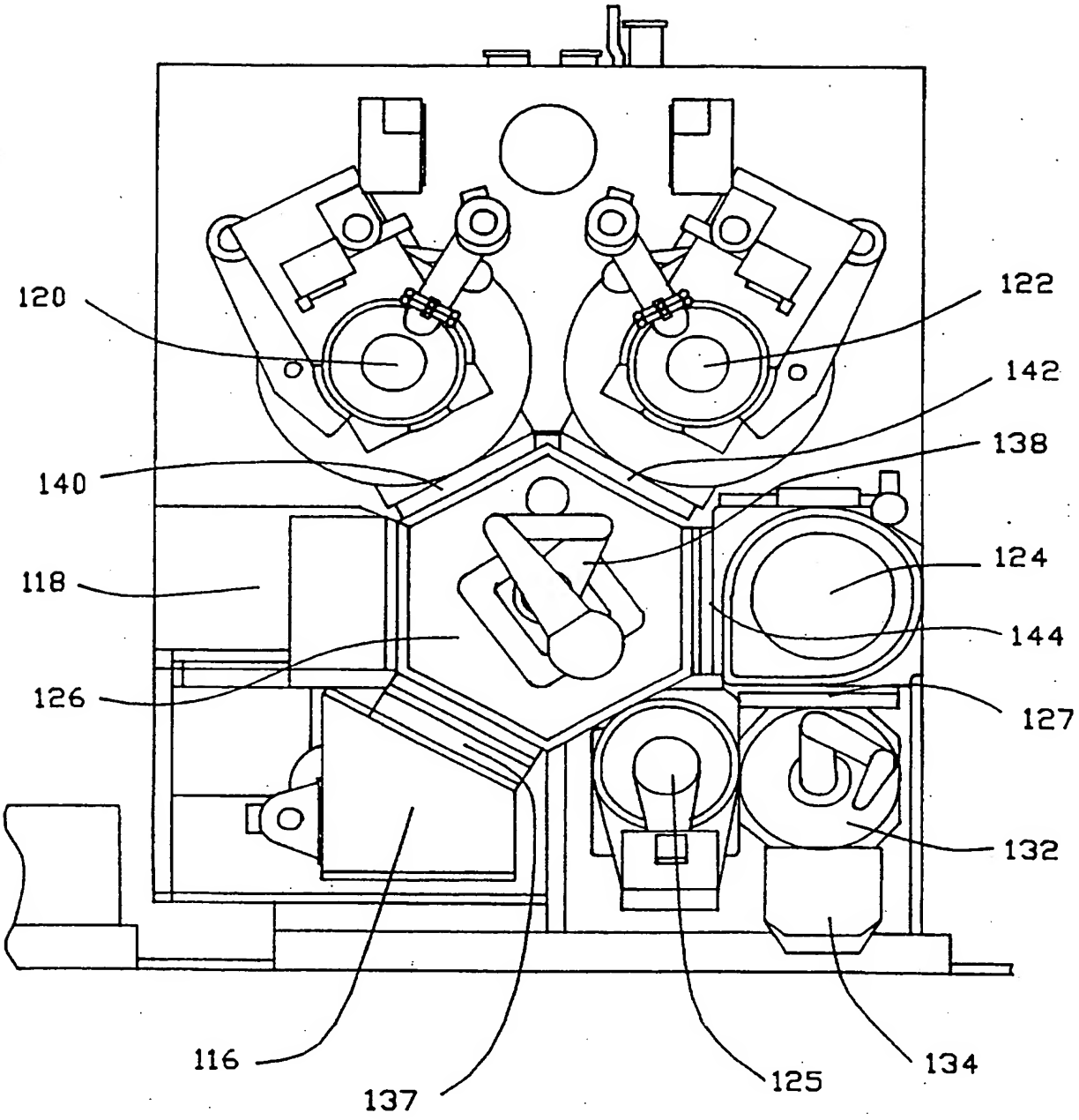

FIG.—13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01002

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/302
US CL :156/345, 643.1, 646.1, 651.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 156/345, 643.1, 646.1, 651.1, 656.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: USPAT; Orbit: WPAT, JAPIO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------- Y	JP, A, 59-016,334 (MATSUSHITA ELECTRONIC CORP) 27 January 1984, abstract.	1, 11, 28 ---------- 2, 4-10, 13-16, 20, 28-31, 35-36, 40, 42-46
A	US, A, 4,902,377 (BERGLUND ET. AL.) 20 February 1990, columns 2-4.	21-27
X ------- Y	US, A, 4,889,588 (FIOR) 26 December 1989, Figures 1-2, columns 2-3.	1, 28 ---------- 4-11, 13, 16, 20, 29-30, 35-36, 40, 43-46

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
08 JULY 1997	23 JUL 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer for GEORGE A. GOUDREAU Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01002

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,565,036 (WESTENDORP ET. AL.), 15 October 1996, Figure 7, columns 10-11.	1-46
X	US, A 5,498,768 (Nishitani et. al.), 12 March 1996, Figures 1, 12, columns 8-11.	1, 28
Y		2, 4, 10-11, 13, 19, 29, 30, 35, 40, 43-46